APPARATUS, METHODS AND ARTICLES OF MANUFACTURE FOR SIGNAL CORRECTION USING ADAPTIVE PHASE RE-ALIGNMENT

FIELD OF THE INVENTION

[0001]   The invention relates generally to electromagnetic processing, and more particularly, the invention relates to signal correction using adaptive phase re-alignment.

BACKGROUND OF THE INVENTION

[0002]   Correcting errors that occur during the processing of electromagnetic waves and signals (hereinafter "waves") is sometimes difficult.   These waves may be used for many different purposes.   For example, they may be processed in order to convey intelligence, such as by attenuating and/or amplifying electromagnetic wave characteristics, for instance, as is seen when modulating amplitude, frequency or phase of an electrical current or radio frequency (RF) wave to transmit data.   As another example, power may be conveyed along a wave in a controlled fashion by attenuating and/or amplifying electromagnetic wave characteristics, such as is seen when modulating voltage or current in a circuit.   Moreover, the uses may be combined, such as when intelligence may be conveyed through a wave by processing power characteristics.

[0003]   Because low frequency waves, such as 60 Hz power waves, may need different processing techniques than high frequency waves such as 24 GHz radar waves, it is common practice to use different components, with different characteristics, for different waves.   For example, a switching semiconductor used within a computer for 60 Hz power waves has different power handling characteristics from a power semiconductor used in a 24 GHz radar system.   Each of these systems may produce errors in the processed signal, however, due to

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errors that may be introduced into some of the characteristics of the electromagnetic wave during signal processing.

[0004]   For example, in phase modulation systems, errors may occur in the phase of the output signal from errors introduced during the modulation process. In these wave processing systems and others, the processing system must oftentimes be calibrated during manufacturing and/or at periodic intervals during use to reduce the errors introduced into the signal during processing. Calibrating the processing system in this way requires that a system be taken out of service or causes delay and expense in manufacturing the system.

[0005]   Thus, it would be beneficial to calibrate the system by adaptively processing in an ongoing basis during operation, to closely re-produce the desired characteristics of the electromagnetic input wave with predetermined (e.g., idealized) wave characteristics during wave processing. Accordingly, it would be helpful to the art of electromagnetic processing to provide efficient, and at the same time, accurate techniques for correcting electromagnetic waves during signal processing.

SUMMARY OF THE INVENTION

[0006]   Embodiments of the invention include apparatus, methods and articles of manufacture for automatically adapting electromagnetic waves during signal processing. The invention may include a system for adaptively re-aligning a modulated output signal having an error component by generating a reference phase signal using a phase input signal; generating a sample phase signal from the output signal; comparing the reference and sample signals; and adaptively re-aligning any difference between the reference and sample signals to substantially reduce the error component.

[0007] The invention may also incorporate a sampling circuit for sampling the output signal to generate the sample signal; a digital phase locked loop for combining the phase input signal with a carrier wave to generate the reference signal and comparing them to generate a phase error signal; a reference filter for generating reference phase error information; a combining circuit for combining the phase error signal with the reference phase error information to generate a correction signal; and an adaptive gain control circuit for adaptively controlling gain in the correction signal to generate a final estimated error used to re-align the output signal with the phase input signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The invention will be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0009] Figure 1 is a schematic diagram illustrating an adaptive phase re-alignment circuit;

[0010] Figure 2 is a block diagram illustrating a transmitter;

[0011] Figure 3 is a block diagram illustrating a phase modulation system; and

[0012] Figure 4 is a chart illustrating simulated performance results for the embodiment of the invention disclosed herein.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Embodiments of the invention include apparatus, methods and articles of manufacture for adaptively correcting electromagnetic waves during signal processing. For illustration purposes, one embodiment comprises an adaptive phase re-alignment component tailored for tightly matching an input signal to a wideband phase modulator to predetermined wave

characteristics. The system disclosed herein may be used, however, with a wide range of wave

processing systems and is not limited to phase correction or phase modulation systems. The

system may also be used in a wide range of applications, such as, for example, receivers,

transducers, and the like, and is not limited to transmitters.

[0014] The term "signal" as is used herein should be broadly construed to include any manner

of conveying data from one place to another, such as, for example, an electric current or

electromagnetic field, including without limitation, a direct current that is switched on and off or

an alternating-current or electromagnetic carrier that contains one or more data streams. Data, for

example, may be superimposed on a carrier current or wave by means of modulation, which may

be accomplished in analog or digital form. The term "data" as used herein should also be broadly

construed to comprise any type of intelligence or other information, such as, for example and

without limitation, audio, such as voice, text and/or video, etc.

[0015] An embodiment of an adaptive phase re-alignment system is illustrated in detail in

Figure 1. As should be understood, other suitable embodiments for the invention may also be

utilized where desired. In this embodiment, adaptive phase re-alignment component 103 may

include, for example, a radio frequency ("RF") phase quantizer 148, a digital phase lock loop

(DPLL) 140, a reference error filter 142, and an adaptive gain control 146. This embodiment

may be used, for example, to adaptively re-align the phase characteristic of a signal wave as it is

being processed, without the need to disrupt operation of the processing system to calibrate the

system components.

[0016] DPLL 140 may operate, for example, to align the phase of a phase modulated RF

carrier wave with a predetermined "ideal" (i.e., correct) phase by removing any constant phase

offset and/or random frequency drift in the processed signal. For example, where processing

system 150 is a wideband phase modulation system, a phase modulated output signal may be represented by the equation:

$$RF\_VCO\_Out = \cos(\omega_c t + K_{tot}(1+\delta)\sum_n d_n \int_{-\infty}^{t-nT} g(\tau)d\tau + \omega_{drift} t + \Phi) \qquad \text{Eq. 1}$$

where ω_c is center frequency or channel of the carrier wave, $K_{tot}(1 + \delta)$ is the gain error of the processing system, Φ is any constant phase offset and ω_{drift} is any random frequency drift in the modulated signal.

[0017]   An "ideal" reference carrier wave signal may be produced by combining the phase data from a baseband input signal with the center frequency of the carrier wave signal channel, ω_c, calculated by a standard reference source 162. In one embodiment, the baseband input signal may be passed through low pass filter 168 having a response determined by the frequency response of processing system 150 in producing the processed signal.

[0018]   While this carrier wave signal may be a digital value representing the fractional value of the channel in this embodiment, those of ordinary skill in the art will appreciate that it is not limited thereto. The number of bits used to produce the center channel frequency is not particularly limited.

[0019]   This signal may be used to drive phase accumulator 164 in a conventional manner to produce a reference signal representative of the "ideal" phase for the processed output signal (a phase modulated signal in this example). Those of ordinary skill in the art will appreciate that the number of bits used in phase accumulator 164 is not particularly limited. In the illustrated embodiment, the resolution of phase accumulator 164 (i.e, the number of bits) may be equal to that of quantizer 148.

[0020] Quantizer 148, in turn, may be used to sample the signal being outputted from the processing system 150, such as by digitally sampling a phase modulated RF carrier wave signal to extract the baseband phase information for the signal. This function may be accomplished in any number of ways, such as by using an A/D converter, which would output a digital signal from quantizer 148 that contains the phase information of the modulated signal. Quantizer 148 may use a timing signal from clock 152 in a conventional manner. The timing signal from clock 152 may also be incorporated into the digital signal outputted from quantizer 148.

[0021] In one embodiment, quantizer 148 may include a digital prescaler to divide down the RF carrier signal (e.g., by 4), and to simultaneously provide I and Q data. The I,Q data for the phase information in the RF output signal may be quantized to two bits, one for each channel, although the invention is not limited thereto. In addition, the RF carrier signal may be sampled directly to increase the resolution of the sampled signal, thus reducing the impact of quantization noise on the sampled signal. For example, the RF output signal may be combined with the I,Q data to produce a three bit sampled signal i.e., identifying eight phase sectors. In an alternate embodiment, the rising and falling edges of the RF output signal may be used to generate two sets of I and Q signals (offset by half cycle) which similarly increases the resolution of the sampled signal to eight phase sectors. As noted above, the same level of resolution maybe also be used in phase accumulator 164.

[0022] This digital output from quantizer 148 may then be inputted to DPLL 140 for comparison with the "ideal" reference phase signal. For example, this digital signal may be subtracted from the "ideal" reference phase signal at subtractor 154. Subtractor 154 may digitally sum these two signals to produce an output that is thus a phase error signal,

representative of the difference, or error, between the processed output signal wave inputted into

quantizer 148 and the predetermined reference "ideal"signal.

[0023]   The phase wrap 144 ensures that the phase difference does not exceed 2 pi radians (-pi

to +pi). Angles that exceed +/- pi are mapped to corresponding angles in that range, as is

commonly known to those skilled in the art. In one embodiment, carrier phase wrap 144 may

comprise a circuit which performs a modulo 2 operation on the phase error signal if phase error

signal has been scaled down to be between ±1. The circuit may ignore any overflow bits. This

embodiment allows for the modulo 2 operation to be used to flip errors outside this range in sign

and add them (e.g., a value of 1.5 becomes –0.5 and a value of –1.5 becomes +0.5).

[0024]   The output of phase wrap 144 may be passed to decimator 156, which may be used to

reduce the sample rate of the DPLL (e.g., by 32, although not limited thereto). Decimator 156

may comprise, for example a cascaded integrator-comb filter (CIC) type, but is not limited

thereto. Decimator 156 then feeds loop filter 158, which may comprise, for example an FIR

filter having a predetermined response calculated for use with the signal being processed. The

feedback output signal of loop filter 158 may then be combined with the "ideal" reference signal

at subtractor 160.

[0025]   This process allows DPLL 140 to detect and eliminate both the constant phase offset

and small carrier frequency variations in the ideal carrier phase and frequency that may occur.

[0026]   Reference error filter 142 may be operated to produce a reference phase-error

waveform using the phase data of the input signal being processed by the system.   This

reference error signal may serve as a basis function for the measured true phase error. The true

phase error signal from phase wrap 144 may be projected onto this reference error signal at

multiplier 166 to produce an estimated gain error of the PLL. Those of ordinary skill in the art

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will appreciate that a delay may be used to align the true phase error signal to the reference error signal samples.

[0027]   The estimated gain error signal may then be passed, for example, to adaptive gain control and filter 146, which produces the final estimated gain error (δ in sample equation 1) to be used to adaptively re-align the phase of the processed output signal (RF_VCO_Out in sample equation 1). For example, gain may be varied in fixed time steps to achieve fast settling time of the final estimated gain error. In another example, the gain applied in 146 may be adaptively varied based upon the measured error signal. These are advantageous in some modulation schemes, such as CDMA, which have specific, faster requirements for the settling time of the signal.

[0028]   In this way, adaptive phase re-alignment component 103 may be used to re-align the phase of the processed signal. Adaptive phase re-alignment component 103 may measure the output phase of the processing system and compare it to a theoretically perfect ("ideal") version that is derived from the phase and frequency data of the input signal being processed. The result of this comparison is used to adaptively adjust the processing system, eliminating the need to manually calibrate the system components. One example of this is described in more detail below. This feedback system operates to minimize the error in the processed signal.

[0029]   For purposes of illustration of the operation of the invention, a signal transmitter is disclosed in Figure 2, which incorporates an adaptive phase re-alignment system used in connection with a wideband phase modulator in accordance with an embodiment of the invention. The transmitter 10 illustrated in Figure 2 may include, for example, a baseband processor 100 adapted for receiving an input signal, an amplitude/phase signal processor 101,

wideband modulator 102, adaptive phase re-alignment component 103, power amplifier 104 and one or more load lines 105 connected to an antenna.

[0030] Baseband processor 100 may be, for example, a digital signal processor capable of generating a power control signal and a data control signal in response to the input signal, which may be, for example, a baseband signal. The data control signal may be passed from baseband processor 100 to amplitude/phase signal processor 101. In one embodiment, I,Q data may be converted by amplitude/phase signal processor 101 into an analog or digital data control signal that contains the amplitude wave characteristic of the input signal ("A_m"), and an electromagnetic signal that contains the phase wave characteristic of the input signal ("A_p").

[0031] The phase characteristic, A_p, in turn, may be processed separately and then applied to power amplifier 104. For example, phase signal A_p may be passed to wideband phase modulator 102, where the phase characteristic information may be modulated onto a carrier signal in the manner previously described and then sent to power amplifier 104, where it may be regulated by the data control signal A_m in order to generate an output signal for transmission that is an amplified version of the input signal.

[0032] Adaptive phase re-alignment component 103 may receive the phase and frequency information from amplitude/phase signal processor 101, as well as the signal outputted from wideband phase modulator 102. The phase/frequency information may be used in the manner described above to determine an "ideal" phase signal. The output signal from phase modulator 102 may be sampled and compared with this "ideal" phase signal to create a feedback signal for re-aligning phase modulator 102, as described in more detail below.

[0033] An embodiment of a phase modulation system incorporating the invention is further illustrated in Figure 3. In one embodiment, for example, I,Q data may be converted by

amplitude/phase signal processor 101 into a polar signal to create an analog or digital data

control signal that contains the amplitude wave characteristic of the input signal ("A_m"), and an

electromagnetic signal that contains the phase wave characteristic of the input signal ("A_p").

[0034] For example, a rectangular to polar converter may be used to output polar coordinates

in the form (R, theta) where the R coordinate represents the amplitude characteristic of the wave,

and the theta coordinate represents the phase characteristic of the wave.

[0035] The amplitude characteristics, A_m, of the original input signal may be modulated as a

control signal, such as a series of digital pulses comprising a digital word of varying lengths in

various embodiments, which is used to control the amplification in power amplifier 104 of the

signal outputted from phase modulator 102. The phase data from the input signal, A_p, may, in

turn, be first passed through a data scaling processor 120, which scales amplitude of the data

signal appropriately. The change in signal amplitude produced by data scaling processor 120

may be calculated to compensate for any unwanted gain that may be introduced in the output

signal from wideband modulator 102. The scaling of the signal may be accomplished through

any conventional means compatible with the data format. For example, if the phase data signal

is digital, scaling may be accomplished by digital processing. In this embodiment, wideband

modulator 102 is inherently a frequency modulator, so that translation of data for frequency and

phase representations of the data occurs via $d\theta/dt$ 123 shown in Figure 3.

[0036] The phase component signal may then be passed through a modulation compensation

(equalization) filter 121, which is calculated to have a magnitude and phase response that is the

inverse of the closed loop response of wideband modulator 102. As will be discussed below, in

some instances, modulator 102 has an inherent design bandwidth to minimize noise in the signal.

Limiting of the bandwidth in this manner, however, may cause a roll-off, that is, diminution, of

the higher frequency components of the signal. Equalization filter 121 and overall modulation response filter 122 compensates for roll-off by increasing the gain of these higher frequency components, thus producing a more even (flattened) frequency response for the system and effectively extending the modulation bandwidth of wideband modulator 102.

[0037] The equalization filter 121 is preferably implemented digitally, using a digital signal processor, although not limited thereto, and may be either a FIR (finite impulse response) or IIR (infinite frequency response) filter, as examples. The phase component data may also be passed through overall modulation response filter 122, which is calculated to set the overall passband response of wideband modulator 102 (e.g., 4MHz). Overall modulation response filter 122, similar to equalization filter 121, may be an analog or digital FIR or IIR filter. Functionally, filters 121 and 122 may be combined into a single filter where desired.

[0038] In the embodiment disclosed herein, the baseband input signal may be modulated onto a carrier wave of a selected center frequency in wideband modulator 102. The center frequency about which a given signal is to be modulated is determined by a channel calculation, by which the carrier wave frequency (e.g., 1880 MHz) is divided by the frequency of the reference source to establish a channel for the signal.

[0039] In this embodiment, the channel calculation yields a number that has an integer part and a fractional part. As shown in Figure 3, channel calculator 124 received the channel number from baseband processor 100 and determines a selectable non-whole number (e.g., 23.5 to 24.5) by which the carrier wave of wideband modulator 102 is to be divided, allowing the selection of a channel in which the phase data signal is to be modulated. The fractional portion of this number may then combined with the data signal, which is passed to sigma delta modulator

(SDM) 125 in wideband modulator 102. (This fractional portion may also be used to provide

channel information to adaptive phase re-alignment component 103, as well).

[0040]   SDM 125 may be used in connection with phase-locked loop (PLL) 126 to achieve

wideband modulation of the input signal onto a carrier wave. SDM 125 serves to randomize and

oversample the inputted phase data, with the average of multiple samples of the output being

equal to the input. The SDM 125 in this embodiment operates in a manner so that inherent

quantization noise from the digitizing process may be frequency shaped, so that at the desired

frequencies, the noise is low.

[0041]   SDM 125 may comprise, for example, a series of adders/accumulators and feedback

components for inputting the fractional phase/channel number data (which may be an analog or

digital signal) and outputting a digitized series of integers that correspond to the fractional input.

The SDM 125 may be configured so that the input range is sufficient for phase modulation data

as well as the fractional portion of the channel number. For example, SDM 125 may be a three

bit system, which is thus capable of producing eight different output numbers (e.g., -3, -2, -1, 0,

1, 2, 3, and 4), although as should be understood, SDM 125 may comprise any desired number of

bits or elements. SDM 125 may produce four output integers for each sample of the input,

yielding an oversampling rate of four times the input. Sampling of the input modulating data in

SDM 125 in this manner may introduce noise on the input modulating signal. Any such noise

may be filtered by low-pass loop filter 131 in PLL 126. The circuit topology for SDM 125 is not

particularly limited, but may include a MASH III topology or a 3rd Order Loop topology, for

example. As should be understood, however, other suitable circuit topologies may also be

utilized for the SDM 125 where desired.

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[0042]   The output of SDM 125 in the illustrated embodiment may then be combined with the integer portion of the channel number received from channel calculator 124. In the example discussed herein, the combination would produce a number from 20 to 28. The combination of the fractional and integer portions of the channel number may be inputted to divider 128 in this embodiment and used to lock PLL 126 to the desired RF carrier.

[0043]   The PLL 126 in the illustrated embodiment may be used to modulate a wave signal synthesized by an RF carrier wave signal source, such as carrier wave source 129, using the phase portion of the input signal. Carrier wave source 129 may be any source of electromagnetic waves that is capable for producing a carrier wave, such as a radio frequency voltage-controlled oscillator (VCO).

[0044]   The frequency of reference source 127 (or a division thereof by some number) may be compared with the output frequency of carrier wave source 129, divided by the series of numbers received by divider 128 from SDM 125 and channel calculator 124. Reference source 127 may comprise a VCO of a constant or substantially constant frequency or may be derived from a source at another frequency.

[0045]   Phase-frequency detector (PFD) 130 may be used to compare the relative phases of the two signals and then output a signal that is proportional to the difference (phase shift) between them. This output signal may be utilized to adjust the frequency of carrier wave source 129, so that the phase difference measured at PFD 130 is substantially close and preferably equal to zero. Hence, the phase of the signal is locked by the feedback loop to prevent unwanted drift of the signal phase, due to variations in the phase and frequency of carrier wave source 129.

[0046]   A feedback signal from carrier wave source 129 may be passed through divider 128, with the division ratio of the divider controlled by the series of numbers representing the phase

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component information received from SDM 125 and the channel information received from

channel calculator 124. The resulting signal may be passed to PFD 130, where it is compared

with the signal from reference source 127, as noted above. This combined signal may be passed

through low-pass loop filter 131, and combined with the carrier wave signal of carrier wave

source 129.

[0047] SDM 125 is being utilized to perform wideband modulation of the phase data input to

SDM 125. Since the phase data input to SDM 125 may not be constant, synchronizing SDM 125

to the output of divider 128 may introduce a frequency offset that is dependent on the modulation

signal. Accordingly, it may be desired in certain embodiments that SDM 125 and divider 128 be

synchronized by reference source 127

[0048] Before the equalization filter 121, the phase characteristic information A_p may be sent

to adaptive phase re-alignment component 103 to be used in phase re-alignment in the manner

previously described. In one embodiment, the phase characteristic information Ap is passed

through Reference Error Filter 142, which is calculated based upon the transfer function of phase

modulator 102 and the equalization filter 121.

[0049] For example, adaptive phase re-alignment component 103 may be used to dynamically

adjust the PLL response, to ensure that the equalization filter 121 and the closed loop response of

the PLL 126 are closely matched. Adaptive phase re-alignment component 103 may measure the

output phase of wideband modulator 102 and compare it to a theoretically perfect version that is

derived from the baseband input data and the center frequency information received from

channel calculator 124. The result of this comparison is used to adjust the loop gain of PLL 126

in wideband modulator 102. This feedback system operates to minimize the error in the

transmitted signal. Adaptive phase re-alignment component 103 preferably operates while the PLL is in service and reduces the need for manual calibration of the system.

[0050] In some embodiments, for example, with certain transmitter, receiver, and transceiver embodiments, the components described herein may be specialized for particular input signals, carrier waves and output signals, e.g. various types of cell phones, such as CDMA, CDMA2000, W-CDMA, GSM, TDMA, as well as various other types of devices, both wired and wireless, e.g. Bluetooth, 802.11a, -b, -g, radar, 1xRTT, radios, GPRS, computers and computer or non-computer communication devices, handheld devices, etc. The modulation scheme that may be used in implementations of the invention is not limited and may include, for example, GMSK, which is used in GSM; GFSK, which is used in DECT & Bluetooth; 8-PSK, which is used in EDGE; OQPSK & HPSK, which are used in IS-2000; p/4 DQPSK, which is used in TDMA; and OFDM, which is used in 802.11.

[0051] Embodiments may utilize both analog and digital components, where desired, insofar as these embodiments manipulate waves and signals requiring both. For example, cell phone embodiments may utilize both analog and digital components. Various types of system architectures may also be utilized for constructing the embodiments. For example, embodiments or various components may be provided on a semiconductor device where desired, such as an integrated circuit or an application-specific integrated circuit composition; some examples include silicon (Si), silicon germanium (SiGe) or gallium arsenide (GaAs) substrates.

[0052] Figure 4 illustrates performance information for a computer generated model of the above-described embodiment of the invention. In this example, adaptive phase re-alignment component 103 was configured to have bandwidth of 100Hz for loop filter 158, an error gain factor of $1 \times e^{-6}$, a 4 bit accumulator and quantizer 164, and a 2 bit phase quantizer,

148.Adaptive phase re-alignment was simulated using a phase delta gain error factor of –0.4, –

0.2, 0, +0.2, and +0.4. As shown in Figure 4, the system corrected for these gain errors up to

about 40% with about 0.1% residual error.

[0053] Having thus described a few particular embodiments of the invention, various

alterations, modifications, and improvements will readily occur to those skilled in the art. Such

alterations, modifications and improvements as are made obvious by this disclosure are intended

to be part of this description though not expressly stated herein, and are intended to be within the

spirit and scope of the invention. One of ordinary skill in the art will accordingly appreciate that

embodiments of the invention or various components and/or features thereof may be entirely

comprised of hardware, software and/or may be a combination of software and hardware.

Accordingly each of the blocks of the drawings, and combinations of blocks of the drawings,

may be embodied in many different ways, as is well known to those of skill in the art.

Accordingly, the foregoing description is by way of example only, and not limiting. The

invention is limited only as defined in the following claims and equivalents thereto.